simplified, the number of the circuit elements can be reduced, and the lower power consumption can be achieved.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

What is claimed is:

1. A video signal control circuit that processes a video signal of which one line is composed of plural pixels as an input data, comprising:

a delay circuit that receives the input data, and delays the input data to thereby output as plural output signals, wherein a delay of the delay circuit is selectively variable;

a counter circuit that counts a pixel number of each line in the input data; and

a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates

a new delay in accordance with the delay set by the delay circuit and the delay on the basis of the calculated difference;

wherein the delay circuit delays the input signal by the delay selected on the basis of the delay calculated by the judgment circuit.

2. A video signal control circuit as claimed in Claim 1, wherein the delay circuit includes plural flip-flop circuits, and the plural flip-flop circuits convert the pixels constituting the input data into plural output data with each delayed by one clock.

3. A video signal control circuit as claimed in Claim 2, wherein the judgment circuit possesses a selector that selects, on the basis of the calculated delay, a corresponding data out of the plural output data from the delay circuit.

4. A video signal control circuit as claimed in Claim 1, wherein the judgment circuit is able to set an initial value of the delay to the delay circuit in accordance with a selection signal.

5. A video signal control circuit as claimed in Claim 4, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial delay in accordance with the inclination of the pixel dispersion.

6. A video signal control circuit that processes a video signal of which one line is composed of plural pixels as an input data, comprising:

a memory circuit which the input data can be written in and read from, which includes two one-port memories, wherein the input data are alternately written in the two one-port memories, and the written input data are alternately read from the two one-port memories;

an address generation circuit that outputs a write address or a read address to the memory circuit;

a counter circuit that counts a pixel number of each line in the input data; and

a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates

a new address value in accordance with an address value generated by the address generation circuit and a delay based on the calculated difference;

wherein the address generation circuit generates the write address signal or the read address signal on the basis of the address value calculated by the judgment circuit, and when there is a difference between the pixel number of the input data read from the one-port memory and that of the input data written in the one-port memory, some of the plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers.

7. A video signal control circuit that processes a video signal of which one line is composed of plural pixels as an input data, comprising:

a memory circuit including a two-port memory that is able to write in

and read out the input data in parallel;

an address generation circuit that outputs a write address or a read address to the memory circuit;

a counter circuit that counts a pixel number of each line in the input data; and

a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates

a new address value in accordance with an address value generated by the address generation circuit and a delay on the basis of the calculated difference;

wherein the address generation circuit generates the write address signal or the read address signal on the basis of the address value calculated by the judgment circuit, and when there is a difference between the pixel number of the input data read from the memory circuit and that of the input data written in the memory circuit, some of the plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers.

8. A video signal control circuit as claimed in Claim 6, wherein the repetition processing or the deletion processing in the address generation circuit is executed to a rear part of the line of the input data.

9. A video signal control circuit as claimed in Claim 7, wherein the repetition processing or the deletion processing in the address generation circuit is executed to a rear part of the line of the input data.

10. A video signal control circuit as claimed in Claim 6, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

11. A video signal control circuit as claimed in Claim 10, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion.

12. A video signal control circuit as claimed in Claim 7, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

13. A video signal control circuit as claimed in Claim 12, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion.